EMPC23

What future do you want to connect with?

Programme

24th European Microelectronics & Packaging Conference and Exhibition

12 – 14 September 2023 Cambridge, UK

For more information, visit

empc2023.org

Platinum Sponsor

Besi

Gold Sponsors

Accelonix keeping you ahead.

inseto

PacTech member of nagase group

CONTENT

Co-sponsored by:

IEEE

IEEE ELECTRONICS PACKAGING SOCIETY

Organised by:

iMAPS UNITED KINGDOM

WELCOME TO EMPC 2023

Welcome to the 24th European Micro-electronics Packaging Conference being held at the Wellcome Genome Campus (EMPC 2023). This biennial Conference is organised by IMAPS-UK with the support of IMAPS-Europe and is co-sponsored by the IEEE – Electronics Packaging Society.

The conference will present the latest developments in the field of microelectronics packaging and interconnection technologies from industrial and R&D organisations located across the world. Over 90 abstracts have been organised into 20 sessions and posters over the 3 days of the conference, with ample time for attendees to interact with the exhibitors in the integrated venue. The conference welcomes over 250 attendees from the UK, the rest of Europe and around the world.

The five keynote speakers represent leading edge companies, all pushing the boundaries of what can be achieved with microelectronics packaging in a wide range of applications. We are delighted to welcome Chris Scanlon of BESI, Florin Udrea of Cambridge GaN Devices, Ali Murad of Paragraf, Mark Gerber of ASE Group and Feras Alkhalil of Pragmatic Semiconductor to give their perspective of the challenges faced and solutions delivered in this ever more complex world of microelectronics.

In addition to the comprehensive conference programme of presentations and posters, there are many opportunities to meet with the Exhibitors in the co-located space, who represent the breadth of the microelectronics supply chain. We are particularly grateful for the support of the Platinum sponsor, BESI, the three Gold sponsors – Accelonix, Inseto and PacTech and to ASE Group for sponsoring the welcome reception, the conference dinner and the lanyards.

A ceremony is planned at the close of the conference, where we will present the EMPC 2023 Best Paper and Poster Awards and thank all the authors who presented their work.

The welcome reception and conference dinner will be held in Homerton College in Cambridge. You will have the opportunity to make new contacts and meet old friends in the ambience of a modern collegiate dining room and spacious gardens. We hope that you will also have time to visit the city of Cambridge, with its many historic colleges, museums and art galleries.

Finally I express my most sincere gratitude to the Technical Committee and the EMPC 2023 organising team for supporting the conference, reviewing the papers and helping the EMPC conference maintain its high technical and scientific standards.

WE WISH YOU AN EXCELLENT EMPC 2023 CONFERENCE.

Anne Vanhoestenberghe
and the EMPC2023 organising team

SCIENTIFIC COMMITTEE

Conference Chair:
Anne Vanhoestenberghe, King's College London, UK

Organising Committee:
Stephen Riches, IMAPS-UK, UK
Peter Barnwell, IMAPS-UK Trustee, UK
Andrew Holland, RF Module And Optical Design Limited, UK
John Lipp, IMAPS-UK, UK
Eamonn Redmond, Inseto (UK) Ltd, UK
Martin Wickham, National Physical Laboratory, UK
Scott Wood, Accelonix, UK

Technical Committee:

Hassan Akhtar	Manufacturing Technology Centre, UK
Rolf Aschenbrenner	Fraunhofer IZM, DE
Peter Barnwell	IMAPS-UK Trustee, UK
Derek Braden	Aptiv, UK
Luigi Calligarich	ELECTRON MEC, IT
Jayakrishnan Chandrappan	CSA Catapult, UK
Norocel Codreanu	University POLITEHNICA of Bucharest, RO
Paul Collander	IMAPS Nordic, FI
Suzanne Costello	MCS Ltd, UK
Gerard Cummins	University of Birmingham, UK
Giovanni Delrosso	VTT Technical Research Center of Finland, FI
Bradford Factor	ASE, FR
Attila Géczy	Budapest University of Technology and Economics, HU
Andrew Holland	RF Module And Optical Design Limited, UK
Szendiuch Ivan	Brno University of Technology, CZ
Malgorzata Jacubowska	Warsaw University of Technology, PL
Jeff Kettle	University of Glasgow, UK
David King	Alter Technology, UK
Olivér Krammer	Budapest University of Technology and Economics, HU
John David Lipp	IMAPS-UK, UK
Andy Longford	PandA Europe, UK
Wendy Luiten	WLC, NL
Jens Müller	Technische Universität Ilmenau, DE
Viorel Nicolau	"Dunarea de Jos" University of Galati, RO
Eamonn Redmond	Inseto (UK) Ltd, UK
Stephen Riches	IMAPS-UK, UK
Mark Shaw	STMicroelectronics, IT
Carolyn Short	KLA Corporation, UK
Stoyan Stoyanov	University of Greenwich, UK
Tatjana Trajkovic	Cambridge Microelectronics Ltd, UK
Susan Trulli	Raytheon Missiles and Defense, MA
Martin Wickham	National Physical Laboratory, UK
Scott Wood	Accelonix, UK

KEYNOTE SPEAKERS

KEYNOTE 1
INTERCONNECTING CHIPLETS

Chris Scanlon, Senior Vice President Technology, BESI Switzerland

Abstract

The semiconductor industry is undergoing a shift from traditional transistor scaling to heterogeneous integration (HI) using chiplets. While SoC is becoming infeasible for some applications due to the limitations of Moore's Law, chiplets provide a way to continue system-level scaling through More than Moore. However, chiplet systems can be complex and require a hierarchy of different interconnect types in the same package. The most advanced interconnect technology for chiplets is hybrid bonding, which connects chips directly with Cu-Cu bonds. Die-to-wafer hybrid bonding has already been in volume production since 2022 for high-performance computing (HPC) applications. However, complete HI systems require other advanced wafer-level assembly processes as well, including TCB, fan-out and bridge die attach, wafer-level flip-chip, and wafer molding. In the near future, photonic chiplets will be introduced, and together these interconnect methods can form a hierarchy of interconnect in complex chiplet systems. In this speech we will explore the opportunities and challenges of chiplet integration for continued system-level scaling. We will discuss the different interconnect technologies used in chiplet systems and the advancements in assembly equipment that enable these high density interconnects. We will also examine the importance of collaboration and standardization in the chiplet ecosystem and how they can enable the rapid development of new products and business models.

Biography

Chris Scanlan is Senior Vice President Technology at Besi Switzerland where he is leading advanced technology road map development and technical promotion. Prior to joining Besi he was Vice President of Worldwide Applications Engineering at JCET Group where he was responsible for business development, technical program management and product design. From 2009 to 2019 he was SVP of Product Development at Deca Technologies. Chris was primarily responsible for the development of Deca's portfolio of intellectual property and technology relating to advanced wafer-level manufacturing methods. Chris worked at Amkor Technology for 10 years where he held leadership positions including VPs of Global R&D, Advanced Products and System in Package business units. Chris started his career at Motorola Semiconductor covering manufacturing of high power IGBT modules and transfer of fcCSP technology from R&D to production. He has 70 issued US patents related to semiconductor packaging. He earned his MSc. degree in Materials Engineering from the University of Wisconsin-Milwaukee.

KEYNOTE SPEAKERS

Keynote 2

KEYNOTE: WIDE BANDGAP DEVICES AND MULTI-DIMENSIONAL ARCHITECTURES IN THE NEW ERA OF POWER ELECTRONICS

Professor Florin Udrea, Cambridge GaN Devices, UK

Abstract

The power devices field has seen tremendous changes in the last decade. Most of the innovation in the field comes from the emergence of Wide Bandgap semiconductors – and in particular those based on Gallium Nitride and Silicon Carbide. Extensive research is also carried out in single crystal Diamond, Gallium Oxide and Aluminium Nitride materials. The market of power devices has reached ~$50M with exponential growth in wide bandgap materials reaching CAGRs in excess of 50% in the next 3-5 years. This talk will cover an exciting range of wide bandgap (WBG) and ultra wide bandgap (UWBG) semiconductor technologies and materials for power devices. The talk will also address the new multi-dimensional architectures to further increase efficiency of power semiconductor devices.

Biography

Professor Florin Udrea is a professor in semiconductor engineering and head of the High Voltage Microelectronics and Sensors Laboratory at University of Cambridge. He is currently leading a research group in power semiconductor devices and solid-state sensors that has won an international reputation during the last 25 years. Prof. Udrea has published over 500 papers in journals and international conferences and holds over 200 patents in power semiconductor devices and sensors. Prof. Florin Udrea founded five companies, including Cambridge GaN Devices in high voltage GaN technology. For his 'outstanding personal contribution to British Engineering' he has been awarded the Silver Medal from the Royal Academy of Engineering. In 2015 Prof. Florin Udrea was elected a Fellow of Royal Academy of Engineering. In 2018 Prof. Udrea has been awarded several major prizes, including the Mullard medal from the Royal Society. In 2020 he received the Ohmi award as a co-author of the ISPSD paper on Silicon Carbide FInFETs. In 2021 he was awarded the academic entrepreneur of the year in UK by Business Weekly.

Keynote 3

KEYNOTE: THE CHALLENGES OF INTEGRATING GRAPHENE INTO EXISTING PACKAGES

Dr. Ali Murad, Test & Packaging Engineer. Paragraf, UK

Abstract

Graphene has been one of the most exciting materials in recent years for a wide variety of industries ranging from electronics, energy, medicine, sensors, and many more. It has been referred to as a wonder material due to its incredible mechanical strength, lightness, flexibility, optical transparency, and impressive semiconductor properties (of both electricity and heat). Paragraf is the first company in the world to mass produce graphene-based electronic devices using standard semiconductor manufacturing processes, has been at the forefront of this effort. However, there are industrywide challenges related to graphene which Paragraf continues to overcome. Some of the challenges are, getting high-quality uniform contamination-free graphene, managing device integration to graphene, integrating graphene devices to industry standard packaging etc. This talk will focus on discussing these challenges, including how Paragraf is producing high-volume graphene based devices for industry applications. This talk will also focus on the latest development of Paragraf's technology and how Paragraf is using its technology to solve real-world problems like heat detection in EV batteries, brushless motors, and many more. In summary, this talk is aiming to provide an overview of the challenges of integrating graphene into packages and the role Paragraf is playing in advancing the use of graphene in industrial applications.

Biography

Dr. Ali Murad is a Test and Packaging Engineer at Paragraf Ltd., specializing in nanotechnology and semiconductor packaging. With a distinguished background in the field and experience at Intel Corporation and Nexperia Ltd., Dr. Murad brings extensive industry knowledge and expertise. As a sought-after keynote speaker, he shares valuable insights on the latest advancements and trends in nanotechnology and semiconductor packaging.

KEYNOTE SPEAKERS

Keynote 4

KEYNOTE: ADVANCED PACKAGING - CHALLENGES THAT ARE DRIVING NEW PACKAGE INNOVATION & ECOSYSTEM NEEDS

Mark Gerber, Sr. Director Engineering and Technical Marketing, ASE Group, USA

Abstract

Advanced silicon node challenges, and the drive within industry to find new ways of offering the highest level of performance, are driving many new ways to extend advanced packaging. Many analysts defined advanced packaging as packaging that uses a higher density of interconnect, outside of the traditional wire-bond. This category opens a broad spectrum of packaging solutions that include, Flip Chip, Fan Out Wafer Level Packaging, Hybrid Packaging, System in Package, 2.5D/3D and many sub-categories. As yield enhancement and performance improvements are driving design considerations, such as heterogeneous and homogenous integration, it is becoming more complex to navigate this plethora of new options and to understand the key trade-offs in selecting the right package solution. Challenges including power delivery signal integrity, multi-physics impacts, IP block interface standards, chiplet manufacturing considerations, warpage and many others are driving the ecosystem to change to meet these new and evolving needs. The traditional 2D mindset for silicon integration in packaging is rapidly changing and a 3D or vertical mindset is becoming a key driver for HPC, AI and is extending into mobile products. In this plenary talk, I will discuss these challenges and also talk about some of the solutions as well as needs from the ecosystem to help enable this new era.

Biography

Mark is Sr. Director of Engineering and Marketing at ASE (US) Inc., He manages a team that supports customer activities around the world focused on all market segments with package multiple platform focus areas including Flip Chip, Copper Pillar, Advanced RDL and SiP Packaging Technologies. Mark has +20 years of semiconductor packaging experience working for Advanced Semiconductor Engineering-ASE, Texas Instruments, Motorola and Dallas Semiconductor in various areas of design, manufacturing, and assembly with an emphasis on the development of new technologies and processes. Mark has served as general chair for multiple conferences, led multiple committees for IMAPS and IEEE and is currently serving on the IMAPS executive committee as a director. Mark was awarded the IMAPS Fellow title in 2018. He holds a bachelor's degree in mechanical engineering from Texas A&M University, has written +20 papers and holds 38 semiconductor packaging patents.

Keynote 5

KEYNOTE: REINVENTING ELECTRONICS FOR A SUSTAINABLE WORLD

Dr Feras Alkhalil, Principal Scientist and Director of R&D, Pragmatic Semiconductor, UK

Abstract

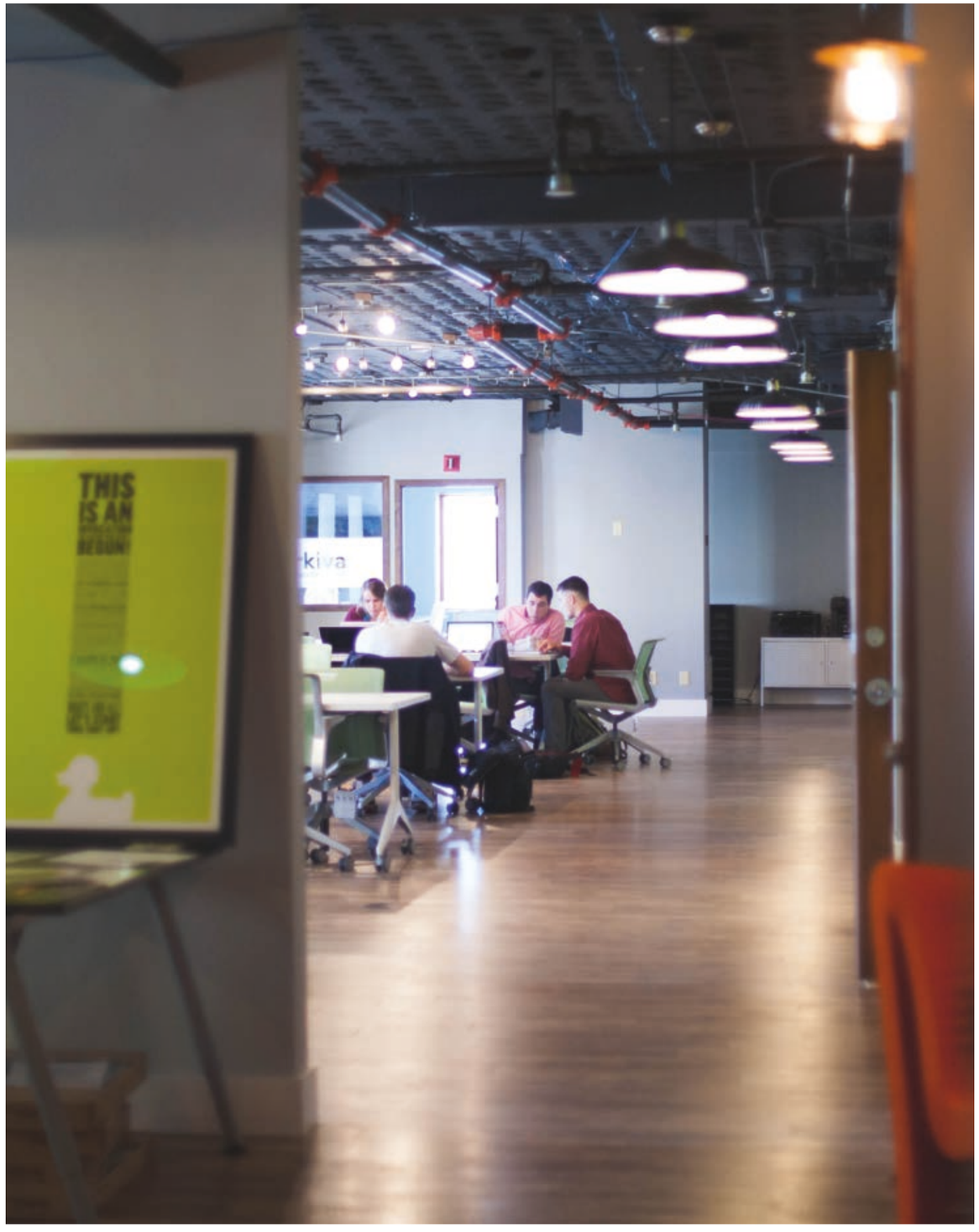
Tackling challenges associated with the climate crisis, sustainability of food supplies and healthcare inequalities require innovative sustainable approaches. Pragmatic Semiconductor is a world leader in the design, development and manufacture of ultra-low-cost Flexible Integrated Circuits (FlexICs). Pragmatic's FlexICs technology is unique in allowing designers to access extremely agile design cycles, coupled with a low cost and low environmental footprint distributed manufacturing model, this enables sustainable democratised innovation. In this session, we will present Pragmatic's innovative FlexIC Foundry™, offering novel form-factor integrated circuits, that can be used to create ubiquitous low-cost smart systems. We will also present novel emerging technologies, that we are currently developing, that will enable designers to create even more innovative designs with Pragmatic's FlexIC Foundry.

Biography

Dr Feras Alkhalil is the Director of R&D at Pragmatic Semiconductor. Feras has been leading the Research and Development activities at Pragmatic since 2015, responsible for early-stage technology development. Feras has an Electronics Engineering background and received an MSc and Ph.D. from the University of Southampton in Microelectronics System Design and Solid-State Quantum Electronics, respectively. Feras taught Semiconductor Physics at the University of Southampton in Malaysia 2013-2015, holds a visiting fellowship with Durham University since 2017, and has more than 10 patents and is published in over 18 international journals.

PRE-CONFERENCE DAY
MONDAY, SEPTEMBER 11, 2023

8:30 am – 6:00 pm	**Pre-Registration**	
9:00 am – 1:00 pm	**SC 1: EVOLUTION OF DIE ATTACH ADHESIVES & ENCAPSULANTS USED IN SEMI-CONDUCTOR PACKAGING** Course instructor: Tony Winster, Henkel Ltd., Germany	**SC 2: FAN-OUT, CHIPLET DESIGN, AND HETEROGENEOUS INTEGRATION PACKAGING** Course instructor: John H. Lau, Unimicron Technology Corporation, USA
1:30 pm – 5:30 pm	**SC 3: POWER ELECTRONICS PACKAGING – UNDERSTANDING THE PACKAGING PROCESSES** Course instructor: Andy Longford, PandA Europe, UK	**SC 4: FROM WAFER TO PANEL LEVEL PACKAGING** Course instructors: Tanja Braun, Markus Wöhrmann, Fraunhofer IZM, Germany
6:00 pm – 7:30 pm	**Welcome Reception at Homerton College and Pre-Conference Registration**	



DAY 1
TUESDAY, SEPTEMBER 12, 2023

8:30 am – 8:55 am	**Registration / Networking**	
8:55 am – 9:10 am	**Welcome & Conference Opening** Chair: Anne Vanhoestenberghe, King's College London	
9:10 am – 9:40 am	KEYNOTE 1: INTERCONNECTING CHIPLETS Chris Scanlon, Senior Vice President Technology, BESI Switzerland	
9:45 am – 10:45 am	S 1A: SUBSTRATES: LTCC AND HTCC	S 1B: EMBEDDING
11:15 am – 12:35 pm	S 2A: INTERCONNECT MATERIALS I	S 2B: MEMS/SENSORS
1:40 pm – 2:10 pm	KEYNOTE 2: WIDE BANDGAP DEVICES AND MULTI-DIMENSIONAL ARCHITECTURES IN THE NEW ERA OF POWER ELECTRONICS Professor Florin Udrea, Cambridge GaN Devices	
2:15 pm – 3:15 pm	S 3A: SUBSTRATES – THICK FILM AND CU INTERCONNECTS	S 3B: ADHESIVES AND ENCAPSULANTS
3:45 pm – 5:05 pm	S 4A: INTERCONNECT MATERIALS II	S 4B: MEDICAL
5:10 pm – 7:00 pm	**Exhibition, Poster, Pizza**	

1A: SUBSTRATES: LTCC AND HTCC

Session Chair: Peter Barnwell, IMAPS-UK Trustee, UK
→ Location: Main Conference Room

9:45 am – 10:05 am

HIGH FREQUENCY BANDWIDTH TRANSITION FOR HTCC HERMETIC PACKAGES

Emad Elrifai
EGIDE, France

10:05 am – 10:25 am

APPLICATION OF REACTIVE BONDING METHODS ON LTCC SUBSTRATES

Erik Wiss[1], Alexander Schulz[2], Adam Yuile[1], Jens Müller[2], Steffen Wiese[1]
[1]Saarland University, Chair of Microintegration and Reliability, Germany; [2]TU Ilmenau, Electronics Technology Group, Germany

10:25 am – 10:45 am

LTCC-BASED CERAMIC SUBSTRATES FOR IDENTIFICATION OF TRUSTWORTHY ELECTRONICS

Uwe Krieger[1], Annett Schroeter[1], Franz Bechtold[1], Gunter Hagen[2], Adrian Goldberg[3]
[1]VIA electronic GmbH, Germany; [2]KMS Technology Center GmbH, Germany; [3]Fraunhofer Institute for Ceramic Technologies and Systems IKTS, Germany

10:45 am – 11:15 am **Break - Exhibition**

1B: EMBEDDING

Chairs: Viorel Nicolau, "Dunarea de Jos" University of Galati, Romania
→ Location: Rosalind Franklin Pavilion

9:45 am – 10:05 am

CONCEPTS FOR REALIZING HIGH-VOLTAGE POWER MODULES BY EMBEDDING OF SIC SEMICONDUCTORS

Lars Böttcher, Andreas Ostmann, Thomas Löher, Manuel Seckel
Fraunhofer IZM, Germany

10:05 am – 10:25 am

CERAMIC EMBEDDING OF SIC-SEMICONDUCTORS USING COFIRING TECHNOLOGY

Steffen Ziesche[1], Jobin Varghese[1], Kathrin Reinhardt[1], Birgit Manhica[1], Andreas Schletz[2]
[1]Fraunhofer IKTS, Germany; [2]Fraunhofer IISB, Germany

10:25 am – 10:45 am

CHARACTERIZATION OF EMBEDDED AND THINNED RF CHIPS

Ran Yin[1,2], Helmuth P. E. Morath[1,3], Christian Hoyer[3], Krzysztof Nieweglowski[1,2], Karsten Meier[2], Karlheinz Bock[1,2]
[1]Centre for Tactile Internet with Human-in-the-Loop (CeTI), Germany; [2]Institute of Electronic Packaging Technology, TU Dresden, Germany; [3]Chair of Circuit Design and Network Theory, TU Dresden, Germany

10:45 am – 11:15 am **Break - Exhibition**

2A: INTERCONNECT MATERIALS I

Session Chair: Rolf Aschenbrenner, Fraunhofer IZM, Germany
→ Location: Main Conference Room

11:15 am – 11:35 am
DEPOSITION OF FINE-PITCH INDIUM BUMPS ON SINGLE DIE
Andreas Schneider[1], Navid Ghorbanian[1], David Burt[2], James Hollingham[1], Paul Booker[1], Toby G. Brookes[1], John D. Lipp[1], Marcus J. French[1]
[1]STFC-RAL, United Kingdom; [2]Kelvin Nanotechnology Ltd., United Kingdom

11:35 am – 11:55 am
SILVER BONDING WIRE – AN ALTERNATIVE FOR MECHANICAL SENSITIVE CHIP CONFIGURATIONS IN AUTOMOTIVE ELECTRONICS PACKAGING
Robert Klengel[1], Sandy Klengel[1], Noritoshi Araki[2], Motoki Eto[2], Teruo Haibara[2], Takashi Yamada[2], Jochen Feldmann[3], Ralph Binner[3], Henk Peters[3], Achim Scheer[3], Vincent Chee[3]
[1]Fraunhofer IMWS, Germany; [2]Nippon Micrometal Corporation, Japan; [3]ELMOS Semiconductor SE, Germany

11:55 am – 12:15 pm
COPPER PUMPING ANALYSIS FOR CU/SIO2 HYBRID BONDING USING IN-SITU SPM IMAGING
Ali Roshanghias[1], Jaroslaw Kaczynski[1], Ude Hangen[2]
[1]Silicon Austria Labs GmbH, Austria; [2]Bruker Nano GmbH, Germany

12:15 pm – 12:35 pm
UNDERSTANDING THE CONTACT RESISTANCE IN AN ACF BONDING
Helge Kristiansen[1], Knut Eilif Aasmundtveit[2], Giang Nghiem[2], Molly Bazilchuk[3]
[1]Conpart AS, Norway; [2]University of South-Eastern Norway, Norway; [3]Ducky AS, Norway

12:35 pm – 1:40 pm
Lunch - Exhibition

2B: MEMS/SENSORS

Session Chair: Andrew Holland, RF Module And Optical Design Ltd., UK
→ Location: Rosalind Franklin Pavilion

11:15 am – 11:35 am
MEMS MIRROR IN HERMETIC PACKAGE FOR ENHANCED PERFORMANCES
Luca Maggi[1], Marco Del Sarto[1], Amedeo Maierna[1], Mark Shaw[1], Roberto Carminati[1], Gianluca Mendicino[1], Davide Rotta[2], Marco Chiesa[2], Aina Serrano[2], Antonella Bogoni[3]
[1]STMicroelectronics, Italy; [2]CamGraPhIC, Italy; [3]Sant'Anna School of Adanced Studies, Italy

11:35 am – 11:55 am
INNOVATIVE SILICON-CERAMIC (SICER) TECHNOLOGY FOR HIGH-STRENGTH PRESSURE SENSOR APPLICATION USING DIFFERENT MANUFACTURING METHODS
Cathleen Kleinholz[1], Michael Fischer[1], Nam Gutzeit[1], Andrea Cyriax[2], Michael Hintz[2], Thomas Ortlepp[2], Jens Müller[1]
[1]Technische Universität Ilmenau, Germany; [2]CiS Forschungsinstitut für Mikrosensorik GmbH, Germany

11:55 am – 12:15 pm
FROM MEMS STRIP TO MEMS UNIT: A COMPREHENSIVE SIMULATION APPROACH TO WARPAGE
Andrea Ratti[1], Daniele Simoncini[1], Annbel Adolfo[2], Marco Del Sarto[1], Patrick Fedeli[1], Alex Gritti[1], Luca Maggi[1], Teresa Napolitano[1], Mark Andrew Shaw[1], Jefferson Talledo[2]
[1]STMicroelectronics, Italy; [2]STMicroelectronics, Philippines

12:15 pm – 12:35 pm
GAS PERMEABLE PROTECTION CAPS FOR WAFER LEVEL CHIP SCALE PACKAGING (WLCSP) OF MEMS ENVIRONMENTAL SENSORS
Ole Behrmann, Thomas Lisec, Björn Gojdka
Fraunhofer ISIT, Germany

12:35 pm – 1:40 pm
Lunch - Exhibition

3A: SUBSTRATES – THICK FILM AND CU INTERCONNECTS

Session Chair: Jens Müller, TU Ilmenau, Germany
→ Location: Main Conference Room

2:15 pm – 2:35 pm

ADDITIVE METALLIZATION OF ALUMINA WITH COPPER-TITANIUM POWDER BLENDS FOR POWER ELECTRONIC APPLICATIONS

Christoph Hecht[1], Eric Schadow[1], Mario Sprenger[1], Felix Häußler[1], Thomas Stoll[2], Jörg Franke[1]
[1]IFriedrich-Alexander-Universtität Erlangen-Nürnberg, Nuremberg, Germany; [2]TUM School of Engineering and Design, Munich, Germany

2:35 pm – 2:55 pm

NEGATIVE-TONE PHOTO-DEFINABLE POLYIMIDE WITH HIGH THERMAL STABILITY AND THICK FILM PROCESSABILITY

Hitoshi Araki, Takayuki Kaneki, Yu Shoji, Chika Hibino
Toray Industries Inc., Japan

2:55 pm – 3:15 pm

DIP BASED ALL CU INTERCONNECTS

Richard Dixon[1], Luca Del Carro[2], Thomas Brunschwiler[2]
[1]Dycotec Materials Ltd, United Kingdom; [2]IBM Research, Zurich, Switzerland

3:15 pm – 3:45 pm **Break - Exhibition**

3B: ADHESIVES AND ENCAPSULANTS

Session Chairs: Eamonn Redmond, Inseto (UK) Ltd, UK
→ Location: Rosalind Franklin Pavilion

2:15 pm – 2:35 pm

EPOXY MOLDING COMPOUND BLEEDING REDUCTION ON SURFACE MOUNT SEMICONDUCTOR DEVICE

Federico Leone[1], Fulvio Viviani[1], Hidetoshi Seki[2], Masami Ishii[2]
[1]STMicroelectronics, Italy; [2]Sumitomo Bakelite Singapore Pte. Ltd, Singapore

2:35 pm – 2:55 pm

INFLUENCE OF THERMALLY AGED UNDERFILL ON FLIP-CHIP PACKAGES

Kevin Cox, Ghassan Abu-Hamdeh, Matt Borden
Tektronix Component Solutions, United States of America

2:55 pm – 3:15 pm

ADHESIVE SOLUTIONS FOR CLOSED CAVITY PACKAGING

Patrick Schirmer, Severin Ringelstetter
DELO Industrie Klebstoffe GmbH & Co. KGaA, Germany

3:15 pm – 3:45 pm **Break - Exhibition**

4A: INTERCONNECT MATERIALS II

Session Chair: Krammer Olivér, BME, Hungary
→ Location: Main Conference Room

3:45 pm – 4:05 pm
DEVELOPMENT OF A STRETCHABLE AND REMOVABLE ELECTRICAL INTERCONNECTION SOLUTION FOR ULTRA-THIN ELECTRONIC COMPONENTS
Auriane Despax-Ferreres[1], Pascal Tiquet[1], Jean-Charles Souriau[2], Vincent Jousseaume[2], Julia De Girolamo[1]
[1]Univ. Grenoble Alpes, CEA, Liten, Grenoble, France; [2]Univ. Grenoble Alpes, CEA, Leti, Grenoble, France

4:05 pm – 4:25 pm
UV LASER COPPER PAD SURFACE EXPOSURE FOR LASER DIRECT STRUCTURING (LDS) OF INTERCONNECTION
Guendalina Catalano, Alessandro Mellina Gottardo, Riccardo Villa
ST microelectronics, Italy

4:25 pm – 4:45 pm
THE FORMATION OF AG NODULES ON FINE AG-SI PARTICLES
Koji Nakayama[1], Minoru Ueshima[2], Masahiko Nishijima[1], Takeshi Sakamoto[2], Chuantong Chen[1], Katsuaki Suganuma[1]
[1]Osaka University, Japan; [2]Daicel Corporation, Japan

4:45 pm – 5:05 pm
FINE PITCH MICRO INDIUM BUMP INTERCONNECT FLIP CHIP BONDING
Travis Scott
Finetech GmbH & Co.KG, Germany

5:10 pm – 7:00 pm **Exhibition, Poster, Pizza**

4B: MEDICAL

Session Chair: Anne Vanhoestenberghe, King's College London, UK
→ Location: Rosalind Franklin Pavilion

3:45 pm – 4:05 pm
INITIAL LIFE TEST OF SILICONE ENCAPSULATED FR4 PRINTED CIRCUIT BOARDS FOR PRE-CLINICAL ACTIVE IMPLANTS
Ishpa Ali[1], Fei Xue[1], Carlos Perez Henriquez[1], Thomas Niederhoffer[1], Ahmad Shah Idil[1], Dai Jiang[2], Henry Thomas Lancashire[1]
[1]Department of Medical Physics and Biomedical Engineering, University College London, London, UK.; [2]Department of Electronic and Electrical Engineering, University College London, London, UK.

4:05 pm – 4:25 pm
VOIDING IN PARYLENE-C ENCAPSULATION OF SURFACE MOUNT LEDS FOR AN OPTOGENETIC EPILEPSY NEUROPROSTHESIS
Ahmad Shah Idil[1], Richard Bailey[2], Johannes Gausden[2], Antony O'Neill[2], Nick Donaldson[1]
[1]University College London, UK; [2]Newcastle University, UK

4:25 pm – 4:45 pm
ASSEMBLY OF PRINTED INTERCONNECTS FOR IMMOBILIZED PROTEIN MICROFLUIDIC ASSAYS
Qianwen Xu[1], Jeffery C. C. Lo[1], Yusong Guo[1], S. W. Ricky Lee[1,2,3]
[1]The Hong Kong University of Science and Technology, Hong Kong, PRC; [2]HKUST Shenzhen-Hong Kong Collaborative Innovation Research Institute, PRC; [3]HKUST LED-FPD Technology R&D Center at Foshan, PRC

4:45 pm – 5:05 pm
FLEXIBLE HYBRID ELECTRONICS ON WEARABLE HEALTHCARE APPLICATION
Ming-Hung Chen
ASE, Taiwan

5:10 pm – 7:00 pm **Exhibition, Poster, Pizza**

POSTER SESSION

01 **TESTING OF ELECTROMIGRATION RESISTANCE OF COPPER AND SILVER THICK FILMS**

Jiri Hlina[1], Jan Reboun[1], Marek Simonovsky[2], Ales Hamacek[1]
[1]University of West Bohemia, Faculty of Electrical Engineering, Czech Republic; [2]Elceram a.s., Hradec Kralove, Czech Republic

02 **RELIABILITY TESTING OF RECYCLED SMD COMPONENTS REUSED IN E-TEXTILES AFTER AGEING BY WASHING CYCLES**

Martin Hirman, Jiří Navrátil, Andrea Benešová, František Steiner
University of West Bohemia, Czech Republic

03 **PROCESS WINDOW OF MINI-LED DISPLAY PANEL PACKAGING USING LASER ASSISTED BONDING TECHNOLOGY**

Yong Sung Eom, Gwang-Mun Choi, Ki-Seok Jang, Ji-Ho Joo, Chan-Mi Lee, Jin-Heuk Oh, Seok-Hwan Moon, Kwang-Seong Choi
ETRI, Republic of South Korea

04 **EFFECT OF SURFACE MICROSTRUCTURE ON JOINTS USING NANOPOROUS CU SHEET FOR POWER DEVICES**

Hiroshi Nishikawa[1], Byungho Park[2], Mikiko Saito[3], Jun Mizuno[3]
[1]Joining and Welding Research Institute, Osaka Universit, Japan; [2]Graduate School of Engineering, Osaka University, Japan; [3]Research Organization for Nano & Life Innovation, Waseda University, Japan

05 **INVESTIGATION OF ALUMINUM AND GOLD FLIP-CHIP BONDING FOR QUANTUM DEVICE INTEGRATION**

Imants Cirulis[1], Uwe Zschenderlein[2], Silvia Braun[1], Moritz Radestock[1], Remi Pantou[1], Klaus Vogel[1], Franz Selbmann[1], Steffen Kurth[1], Bernhard Wunderle[1,2], Harald Kuhn[1,2]
[1]Fraunhofer Institute for Electronic Nano Systems, Germany; [2]Technical University Chemnitz, Germany

06 **ADHESION COPPER/MOLDING COMPOUND: MODELING AND CHARACTERIZATION**
Marco Rovitto[1], Samuele Zalaffi[1], Carlo Passagrilli[1], Claudio Maria Villa[1], Luca Andena[2], Stefano Mariani[2]
[1]STMicroelectronics, Italy; [2]Polytechnic University of Milan, Italy

07 **A HIGH-DENSITY ORGANIC PACKAGE SOLUTION TO W-BAND SIGE FLIP-CHIP APPLICATIONS**
Fırat Altuntaş, Nihan Öznazlı, Olcay Kalkan, Emrah Koç
Aselsan A.Ş, Turkey

08 **THERMAL DESIGN OF STACKED POWER MODULES FOR ELECTRIC DRIVE APPLICATIONS**
Jianfeng Li, Yuekang Du, Xingzhi Wang, Liangjie Liu, Yong Pang, Feixiang Liu
Zhuzhou CRRC Times Electric UK Innovation Centre, United Kingdom

09 **LAMINATION OF CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCER ON A PIEZOELECTRIC ARRAY: PROCESS AND EVALUATION**
Duy Hoang Le, Tung Manh, Lars Hoff
University of South-Eastern Norway (USN), Norway

10 **ASSEMBLY OF ULTRA-THIN MEMS DEVICE ON DRIVER CHIP USING ANISOTROPIC CONDUCTIVE FILM**
Hoang-Vu Nguyen, Knut Eilif Aasmundtveit
University of South-Eastern Norway, Norway

11 **AN INNOVATIVE CONFORMAL ELECTRONICALLY SCANNED ARRAY ANTENNA FOR FULL 360° STEERABILITY IN THE KA-BAND**
Peter Uhlig, Aline Friedrich, Markus Krengel, Winfried Simon, Oliver Litschke
IMST GmbH, Germany

12 **THERMALLY CONDUCTIVE POLYMER COMPOSITES WITH HEXAGONAL BORON NITRIDE FOR MEDICAL DEVICE THERMAL MANAGEMENT**
Nu Bich Duyen Do[1], Kristin Imenes[1], Knut E. Aasmundveit[1], Hoang-Vu Nguyen[1], Erik Andreassen[1,2]
[1]University of South-Eastern Norway, Norway; [2]SINTEF Industry, Norway

13 **MICROSTRUCTURAL BASED RELIABILITY INVESTIGATION OF WATER- AND SUSPENSION FREE PREPARED INTEGRATED ELECTRONIC PACKAGES**
Sandy Klengel, Robert Klengel, Tino Stephan
Fraunhofer IMWS, Germany

14 **NUMERICAL STUDY ON THE INFLUENCE OF POLYIMIDE THICKNESS AND CURING TEMPERATURE ON WAFER BOW IN WAFER LEVEL PACKAGING**
Prashant Kumar Singh[1,2], Patrick Rohlfs[1], Gunther Sandmann[1], Kashi Vishwanath Machani[1], Dirk Breuer[1], Karsten Meier[2], Frank Kuechenmeister[1], Marcel Wieland[1], Karlheinz Bock[2]
[1]GlobalFoundries Dresden Module One LLC & Co. KG, Germany; [2]Technische Universität Dresden, Institute of Electronic Packaging Technology, Germany

15 **IMPROVEMENT OF BONDING STRENGTH AND THERMAL SHOCK RELIABILITY FOR AG SINTER JOINING DIRECT ON AL SUBSTRATE**
Chuantong Chen[1], Ran Liu[1], Koji Kobayashi[2], Hideyo Osanai[2], Zheng Zhang[1], Katsuaki Suganuma[1]
[1]Osaka University; [2]DOWA POWER DEVICE Co., Ltd

16 **INTERCONNECT STRESS TESTING AS A TOOL FOR ASSESSMENT OF RELIABILITY OF MODERN PCB'S**
Marek Koscielski, Krzysztof Glinski, Dariusz Ostaszewski, Tomasz Klej, Jan Oklej, Aneta Cholaj, Wojciech Steplewski, Stefan Galinski
Łukasiewicz Research Network - Tele and Radio Research Institute, Poland

17 **HIGH SPEED TRANSMISSION CHARACTERISTICS ON GLASS BASED INTERPOSERS**
Satoru Kuramochi, Masaya Tanaka, Takahiro Tai
Dai Nippon Printing, Japan

18 **DESIGN, FABRICATION, AND CHARACTERIZATION OF A 4H-SIC CMOS READOUT CIRCUIT FOR MONOLITHIC INTEGRATION WITH SIC SENSORS**
Romina Sattari, Henk van Zeijl van Zeijl, Guoqi Zhang
Department of Microelectronics, Delft University of Technology, The Netherlands

DAY 2
WEDNESDAY, SEPTEMBER 13, 2023

8:30 am – 9:00 am	**Networking**	
9:00 am – 9:10 am	**Welcome: Day 2** Chair: Anne Vanhoestenberghe, King's College London	
9:10 am – 9:40 am	KEYNOTE 3: THE CHALLENGES OF INTEGRATING GRAPHENE INTO EXISTING PACKAGES Dr. Ali Murad, Test & Packaging Engineer. Paragraf, UK	
9:45 am – 10:45 am	S 5A: SINTERING I	S 5B: EQUIPMENT / INSPECTION
11:15 am – 12:35 pm	6A: PHOTONICS AND OPTICS	S 6B: SOLDER / SOLDERING
1:40 pm – 2:10 pm	KEYNOTE 4: ADVANCED PACKAGING - CHALLENGES THAT ARE DRIVING NEW PACKAGE INNOVATION & ECOSYSTEM NEEDS Mark Gerber, Sr. Director Engineering and Technical Marketing, ASE Group	
2:15 pm – 3:15 pm	S 7A: SINTERING II	S 7B: HERMETIC / CONFORMAL COATINGS / TIMs
3:45 pm – 5:05 pm	S 8A: FLIP CHIP	S 8B: RELIABILITY AND SUSTAINABILITY
6:00 pm – 10:00 pm	**Pre-dinner drinks followed by Dinner at Homerton College**	

5A: SINTERING I

Session Chair: Martin Wickham, National Physical Laboratory, UK
→ Location: Main Conference Room

9:45 am – 10:05 am

RELIABILITY OF COPPER SINTERED INTERCONNECTS UNDER EXTREME THERMAL SHOCK CONDITIONS

Sri Krishna Bhogaraju[1], Francesco Ugolini[2], Alessio Greci[2], Gordon Elger[1]
[1]Technische Hochschule Ingolstadt, Germany; [2]AMX Automatrix srl, Italy

10:05 am – 10:25 am

RAPID SINTERING OF INKJET PRINTED CU COMPLEX INKS USING LASER UNDER AIR

Nihesh Mohan[1], Sri Krishna Bhogaraju[1], Juan Ignacio Ahuir-Torres[2], Hiren Kotadia[2,3], Gordon Elger[1]
[1]Institute of Innovative Mobility, Technische Hochschule Ingolstadt, Germany; [2]School of Engineering, Liverpool John Moores University, UK; [3]WMG, University of Warwick, UK

10:25 am – 10:45 am

IMPROVING SEMICONDUCTOR RELIABILITY OF SILVER SINTER DIE ATTACH MATERIALS FOR LARGE DIE ON LEAD FRAME APPLICATIONS

Ruud De Wit[1], Edsger Smits[2]
[1]Henkel Nederland BV, The Netherlands; [2]Chip Integration Technology Center (CITC), The Netherlands

10:45 am – 11:15 am **Break - Exhibition**

5B: EQUIPMENT / INSPECTION

Session Chair: Jeff Kettle, University of Glasgow, UK
→ Location: Rosalind Franklin Pavilion

9:45 am – 10:05 am

PICK AND PLACE OF SENSITIVE CHIPS WITH VACUUM-FREE GECOMER® TOOLS

Lukas Lorenz[1], Thomas Ludewig[1], Kai Swiecinski[1], Henrik Ollmann[2], Amirabbas Razkordanisharahi[2], Volker Bock[1]
[1]Fraunhofer IPMS, Germany; [2]INNOCISE GmbH, Germany

10:05 am – 10:25 am

RESEARCH OF CHIP PLACEMENT ACCURACY FOR FAN-OUT WLP USING A NOVEL SELF-ASSEMBLY STAGE

Tadatomo Yamada, Ken Takano, Toshiaki Menjo, Shinya Takyu
LINTEC Corporation, Japan

10:25 am – 10:45 am

ONE-PROBE NANOPROBING OF POWER DEVICES AND ELECTRONIC PACKAGES

Chengliang Huang[1], Vignesh Viswanathan[1], Greg M. Johnson[2], Andreas Rummel[3], Heiko Stegmann[4], Elliott Andrew[5]
[1]Carl Zeiss Pte Ltd, Singapore; [2]Zeiss Microscopy, United States of America; [3]Kleindiek Nanotechnik, Germany; [4]Zeiss Microscopy, Germany; [5]Zeiss Microscopy, UK

10:45 am – 11:15 am **Break - Exhibition**

6A: PHOTONICS AND OPTICS

Session Chair: Jayakrishnan Chandrappan, CSA Catapult; UK
→ Location: Rosalind Franklin Pavilion

11:15 am – 11:35 am
STUDY OF SPATIAL DISTORTION IN INP NANOPHOTONIC MEMBRANES ON DIFFERENT CARRIER SUBSTRATES
Salim Abdi[1], Aleksandr Zozulia[1], Jeroen Bolk[2], Erik Jan Geluk[2], Yuqing Jiao[1], Kevin Williams[1]
[1]Eindhoven Hendrik Casimir Institute (EHCI), Eindhoven University of Technology; [2]Nanolab@tu/e, Eindhoven University of Technology

11:35 am – 11:55 am
LASER-ASSISTED BONDING APPROACH FOR PHOTONIC INTEGRATION PROCESSES
Aleksandr Vlasov, Topi Uusitalo, Evgenii Lepukhov, Heikki Virtanen, Samu-Pekka Ojanen, Jukka Viheriälä, Mircea Guina
Tampere University, Finland

11:55 am – 12:15 pm
INTEGRATION OF MULTI-LITHOGRAPHY TECHNOLOGIES FOR THE FABRICATION OF FLEXIBLE OPTICAL LINK
Akash Sunilkumar Mistry, Krzysztof Kamil Nieweglowski, Karlheinz Bock
Technical University of Dresden, Germany

12:15 pm – 12:35 pm
HYBRID LITHOGRAPHY FABRICATION OF SINGLE MODE OPTICS FOR SIGNAL REDISTRIBUTION AND COUPLING
David Weyers, Krzysztof Nieweglowski, Karlheinz Bock
Technological University Dresden, Germany

12:35 pm – 1:40 pm
Lunch - Exhibition

6B: SOLDER / SOLDERING

Session Chair: Attila Géczy, BME University, Hungary
→ Location: Main Conference Room

11:15 am – 11:35 am
COMPARING THE SOLDERABILITY OF DIFFERENT SAC0307 COMPOSITE SOLDER PASTES
Balázs Illés[1,2,] Halim Choi[1], Agata Skwarek[2]
[1]Budapest University of Technology and Economics, Hungary; [2]Łukasiewicz Research Network - IMiF, LTCC Technology and Printed Electronics Research Group, Poland

11:35 am – 11:55 am
ANISOTROPIC SOLDER PASTE (ASP) MATERIAL SOLUTION FOR LASER ASSISTED BONDING (LAB) PROCESS
Ki-Seok Jang, Yong-Sung Eom, Gwang-Mun Choi, Ji-Ho Joo, Jin-Hyuk Oh, Chan-Mi Lee, Yoon-Hwan Moon, Seok-Hwan Moon, Kwang-Seong Choi
Electronics and Telecommunication Research Institute, Republic of South Korea

11:55 am – 12:15 pm
DURABILITY OF LEAD-FREE SOLDER INTERCONNECTIONS FOR PRINTED CIRCUIT BOARD APPLICATIONS: COMPARING ENERGY-BASED THERMO-MECHANICAL FATIGUE MODELS
Chien-Ming Huang, Jeffrey W. Herrmann
University of Maryland, United States of America

12:35 pm – 1:40 pm
Lunch - Exhibition

7A: SINTERING II

Session Chair: Andy Longford, PandA Europe; UK
→ Location: Main Conference Room

2:15 pm – 2:35 pm

AN EXPERIMENTAL INVESTIGATION OF A FLEXIBLE SINTERED SILVER JOINT FOR MICRO-JOINING BASED ON A DESIGN OF EXPERIMENTS

Laurent Vivet[1], Lahouari Benabou[2], Olivier Simon[2]
[1]VALEO, THS Material Laboratory, France; [2]UVSQ, University of Paris-Saclay, France

2:35 pm – 2:55 pm

UNDERSTANDING CU SINTERING AND ITS ROLE ON CORROSION BEHAVIOUR FOR HIGH-TEMPERATURE MICROELECTRONIC APPLICATION

Juan Ignacio Ahuir-Torres[1], Sri Krishna Bhogaraju[2], Geoff West[3], Gordon Elger[2], Hiren Kotadia[1,3]
[1]Liverpool John Moores University, UK; [2]Technische Hochschule Ingolstadt, Germany; [3]The University of Warwick, UK

2:55 pm – 3:15 pm

INSPECTION TECHNIQUES USING SCANNING ACOUSTIC MICROSCOPY FOR SILVER SINTERING APPLICATIONS IN POWER ELECTRONIC MODULES

Heaklig Ayala[1,2], Jose Ortiz-Gonzalez[1], Mohamed-Amer Karout[1], James Cotty[2], Tim Rumney[2], Philip Mawby[1]
[1]University of Warwick, United Kingdom; [2]Custom Interconnect Limited, United Kingdom

3:15 pm – 3:45 pm **Break - Exhibition**

7B: HERMETIC/CONFORMAL COATINGS/TIMS

Session Chair: Hassan Akhtar, Manufacturing Technology Centre
→ Location: Rosalind Franklin Pavilion

2:15 pm – 2:35 pm

CHARACTERIZATION OF A NOVEL COST-EFFICIENT AND ENVIRONMENTALLY FRIENDLY GRAPHENE-ENHANCED THERMAL INTERFACE MATERIAL

Sihua Guo[1], Kristoffer Harr (Martinsen)[2], Amos Nkansah[2], Jiajia Chen[1], Zhiyang Shen[1], Murali Murugesan[2], Hongfeng Zhang[2], Lars Almhem[2], Arto Ahtonen[2], Jin Chen[3], Johan Liu[1,4,5]
[1]SMIT Center, Shanghai University, PRC; [2]SHT Smart High-Tech AB, Sweden; [3]Shanghai Ruixi New Materials High Tech Co. Ltd., PRC; [4]Electronics Materials and Systems Laboratory, Chalmers University of Technology, Sweden; [5]School of Energy and Materials Science, Shanghai Poly-Tech University, PRC

2:35 pm – 2:55 pm

EVOLUTION OF GETTER TECHNOLOGY IN ELECTRONIC HERMETIC PACKAGING

Luca Mauri, Giovanni Zafarana, Enea Rizzi, Alessio Corazza
SAES Getters, Italy

2:55 pm – 3:15 pm

ADVANCES IN PARYLENE ADHESIVE BONDING FOR THE REALIZATION OF BIOCOMPATIBLE MICROSYSTEMS

Franz Selbmann[1,2], Frank Roscher[1], Maik Wiemer[1], Harald Kuhn[1,3], Yvonne Joseph[2]
[1]Fraunhofer Institute for Electronic Nano Systems ENAS, Germany; [2]TU Bergakademie Freiberg, Institute for Electronic and Sensor Materials, Germany; [3]TU Chemnitz, Center for Microtechnologies, Germany

3:15 pm – 3:45 pm **Break - Exhibition**

8A: FLIP CHIP

Session Chair: John Lipp, STFC, UK
→ Location: Main Conference Room

3:45 pm – 4:05 pm

FLIP-CHIP INTERCONNECTS BASED ON SINGLE METAL-COATED POLYMER SPHERES

Van Long Huynh, Knut Eilif Aasmundtveit, Hoang-Vu Nguyen
University of South-Eastern Norway, Norway

4:05 pm – 4:25 pm

20µM COPPER MICRO-BUMP BONDING THROUGH A SILVER METALLIZATION FOR ADVANCED PACKAGING UNDER A LOW-PRESSURE CONDITION

Zheng Zhang[1], M.-C. Hsieh[1], A. Suetake[1], H. Yoshida[1], R. Okumuara[1], N. Kagami[1], Kazamasa Okamoto[1], Chuantong Chen[1], Kei Hashi-zume[2], N. Hasegawa[2], R. Yoshida[2], H. Homma[2], K. Suganuma[1]
[1]SANKEN, Osaka University, Japan; [2]Okuno Chemical Industries Co. Ltd,

4:25 pm – 4:45 pm

PRACTICAL RESULTS TO DEMONSTRATE AN INCREASE IN THE RELIABILITY OF FLIP CHIP CONNECTIONS BY ADDING NANO-PARTICLES TO SOLDER

David Harvey[1], Teresa Manzanera[2], Kangkana Baishya[3], Guangming Zhang[1], Mohd Arif Anuar[4], Y. C. Chan[1], Nduka Ekere[1], Derek Braden[5]
[1]Liverpool John Moores University, Liverpool, UK; [2]University of Liverpool, Liverpool, UK; [3]Assam Engineering College, Guwahati, India; [4]UniMAP, Perlis, Malaysia; [5]Aptiv, Coventry, UK

4:45 pm – 5:05 pm

DEVELOPMENT AND CHARACTERIZATIONS OF FINE PITCH FLIP-CHIP INTERCONNECTION USING SILVER SINTERING

Julie Gougeon[1,2], Céline Feautrier[1], Laurent Mendizabal[1], Jean-Charles Souriau1, Mona Tréguer-Delapierre[2]
[1]CEA Leti, France; [2]ICMCB, France

6:00 pm – 10:00 pm **Pre-dinner drinks and Dinner at Homerton College**

8B: RELIABILITY AND SUSTAINABILITY

Session Chair: Derek Braden, Aptiv, UK
→ Location: Rosalind Franklin Pavilion

3:45 pm – 4:05 pm

ANALYSIS OF THE IMPACT OF ENVIRONMENTAL CONDITIONS ON THE RELIABILITY IN 5G PCB ASSEMBLIES

Hans Walter[1], Marius van Dijk[1], Julia-Marie Köszegi[1], Saskia Huber[1], Olaf Wittler[1], Michael Kaiser[1], Martin Schneider-Ramelow[1,2]
[1]Fraunhofer IZM, Germany; [2]Technische Universität Berlin, Germany

4:05 pm – 4:25 pm

EVALUATION OF THE ENVIRONMENTAL IMPACT WITHIN SEMI-CONDUCTOR PACKAGING MATERIALS

Andrew Bainbridge, Lewis Clark, Kathleen Grant, Jeff Kettle
University of Glasgow, United Kingdom

4:25 pm – 4:45 pm

COMBINED MEASUREMENT OF TEMPERATURE AND STRAINING OF A PCB DURING OPERATION USING STEREO DIC AND THERMAL CAMERA

Guven Ogus[1], Lukas Wittevrongel[1], Pascal Lava[1], Alessandro Lambrughi[2], Sam Coppieters[2]
[1]MatchID, Belgium; [2]KU Leuven, Belgium

4:45 pm – 5:05 pm

MEASUREMENT AND SIMULATION OF MECHANICAL STRENGTH OF BACK-END-OF-LINE LAYER IN ADVANCED CMOS DIES

Bart Vandevelde[1], Kevin Cox[2], Reza Moloudi[1], Riet Labie[1], Jason Krantz[2], Matt Borden[2], Kris Vanstreels[1], Mario Gonzalez[1]
[1]imec, Belgium; [2]Tektronix, United States of America

6:00 pm – 10:00 pm **Pre-dinner drinks and Dinner at Homerton College**

DAY 3
THURSDAY, SEPTEMBER 14, 2023

8:30 am – 9:00 am	Networking	
9:00 am – 9:30 am	KEYNOTE 5: REINVENTING ELECTRONICS FOR A SUSTAINABLE WORLD Dr. Feras Alkhalil, Principal Scientist and Director of R&D, Pragmatic Semiconductor, UK	
9:35 am – 10:35 am	S 9A: MACHINE LEARNING	S 9B: SOLAR / SENSORS
11:10 am – 12:30 pm	S 10A: HIGH FREQUENCY	S 10B: POWER MODULES
12:30 pm – 1:00 pm	Closing Session - Awards	
1:00 pm – 2:00 pm	Light Lunch & Exhibition	

9A: MACHINE LEARNING

Session Chair: Stephen Riches, IMAPS-UK; UK
→ Location: Main Conference Room

9:35 am – 9:55 am

APPLICATION OF MACHINE LEARNING METHODS FOR PROCESS OPTIMIZATION IN ELECTRONIC PACKAGING PROCESSES

Corinna Niegisch[1], Sabine Haag[1], Tanja Braun[2], Ole Hölck[2], Martin Schneider-Ramelow[3]
[1]Robert Bosch GmbH, Germany; [2]Fraunhofer IZM Berlin, Germany; [3]Technical University Berlin, Germany

9:55 am – 10:15 am

USING DEEP LEARNING RECONSTRUCTION FOR HIGH THROUGH-PUT AND HIGH-RESOLUTION 3D ANALYSIS OF PACKAGED WAFERS

Allen Gu[1], Andrew Elliott[2], Andriy Andreyev[1], Masako Terada[1], Yanjing Yang[1]
[1]ZEISS Research Microscopy Solutions, United States of America; [2]Carl Zeiss Ltd., United Kingdom

10:15 am – 10:35 am

PARTIAL DISCHARGE CHARACTERIZATION OF CERAMIC POWER ELECTRONICS CIRCUIT CARRIERS ASSISTED BY MACHINE LEARNING

Johannes Drechsel, Lars Rebenklau, Henry Barth
Fraunhofer IKTS, Germany

10:35 am – 11:10 am **Break - Exhibition**

9B: SOLAR / SENSORS

Chairs: Knut E Aasmundtveit, University of South-Eastern Norway, Norway
→ Location: Rosalind Franklin Pavilion

9:35 am – 9:55 am

IMPACT OF PAD LAYOUTS AND SOLDER VOLUME ON SELF-ALIGNMENT OF MICRO SOLAR CELLS

Elisa Kaiser[1], Maike Wiesenfarth[1], Victor Vareilles[2], Henning Helmers[1]
[1]Fraunhofer ISE, Germany; [2]Université Grenoble Alpes, CEA LITEN, France

9:55 am – 10:15 am

NOVEL LOW TEMPERATURE AND LOW PRESSURE SINTERING OF ADAS RADAR SENSOR ANTENNA STACK

Sri Krishna Bhogaraju[1], Dirk Busse[2], Alexander Dahlbüdding[2], Philipp Hadrava[3], Hüseyin Erdogan[3], Gordon Elger[1]
[1]Technische Hochschule Ingolstadt, Germany; [2]Budatec GmbH, Germany; [3]Conti Temic microelectronics GmbH, Germany

Power Session (10B)

10:15 am – 10:35 am

BACCHUS – AN ADAPTABLE FORMAT POWER MODULE FOR LOW VOLUME DESIGNS

Piers Tremlett
Microchip, United Kingdom

10:35 am – 11:10 am **Break - Exhibition**

10A: HIGH FREQUENCY

Session Chair: Ivan Ndip, Fraunhofer IZM | BTU Cottbus-Senftenberg, Germany
→ Location: Main Conference Room

11:10 am – 11:30 am
CHARACTERIZATIONS FOR EWLB (EMBEDDED WAFER LEVEL BALL GRID ARRAY) ANTENNA IN MOLDED PACKAGE INTEGRATIONS IN 77GHZ AUTOMOTIVE APPLICATIONS
M.-C. Hsieh[1], F. Zhang[2], F. Zhu[2], K. Liu[2], L. Chua[3], Y. Lin[3], J. Damalerio[3], Hin Hwa Goh[3], Kai Chong Chan[3], Zihao Chen[4]
[1]JCET Group Co. Ltd., Singapore; [2]Andar Technologies Co., Ltd.; [3]JCET Group Co. Ltd.,, Singapore; [4]Harbin Institute of Technology,Shenzhen, PRC

11:30 am – 11:50 am
A DUAL-BAND DUAL-POLARIZED 2X2 ANTENNA ARRAY WITH BEAMFORMING FOR 5G AIP AND MMWAVE APPLICATIONS
Sheng-Chi Hsieh, Wen-Chun Hsiao, Hong-Sheng Hong-Sheng, Cheng-Yu Ho, Chen-Chao Wang
ASE group /Advanced Semiconductor Engineering, Taiwan

11:50 am – 12:10 pm
ANALYSIS AND CHARACTERIZATION OF CASTELLATED HOLES AS RF INTERCONNECTS FOR MODULAR MILLIMETER-WAVE DEVICES
Paul Perlwitz[1,2], Christian Tschoban[1], Ivan Ndip[1], Harald Pötter[1], Martin Schneider-Ramelow[1,2]
[1]TU Berlin; [2]Fraunhofer IZM, Germany

12:10 pm – 12:30 pm
HIGH-Q KU-BAND MICROSTRIP SPIRAL RESONATOR IN FAN-OUT WAFER-LEVEL PACKAGING TECHNOLOGY FOR VCO APPLICATIONS
M. Chernobryvko[1], M. P. Kaiser[1], K. S. Murugesan[1], D. Kuylenstierna[2], J.-M. Köszegi[1], R. Gernhardt[1], T. Braun[1], I. Ndip[1], M. Schneider-Ramelow[1]
[1]Fraunhofer IZM Berlin, Germany; [2]Chalmers University of Technology, Sweden

12:30 pm – 1:00 pm
Closing session - Awards

1:00 pm – 2:00 pm
Light Lunch & Exhibition

10B: POWER MODULES

Session Chair: Andy Longford, PandA Europe, UK
→ Location: Rosalind Franklin Pavilion

11:10 am – 11:30 am
THERMAL-MECHANICAL ANALYSIS OF A POWER MODULE WITH PARAMETRIC MODEL ORDER REDUCTION
Sheikh Rokibul Hassan[1], Pushparajah Rajaguru[1], Stoyan Stoyanov[1], Christopher Bailey[2]
[1]University of Greenwich, United Kingdom; [2]School of Electrical, Computer and Energy Engineering, Arizona State University, USA

11:30 am – 11:50 am
THICKNESS EFFECT OF COPPER CLIPS ON POWER MODULE PACKAGING DESIGN
H. Wan[1], N. Iosifidis[1], X. Zhang[1], R. Rong[2], M. Antoniou[1], P. Mawby[1]
[1]University of Warwick, United Kingdom; [2]MacMic Science & Technology Co., Ltd, China

11:50 am – 12:10 pm
HIGH FREQUENCY THIN FILM MAGNETICS-ON-SILICON WITH IMPROVED INDUCTANCE AND RESISTANCE
Martin Sittner
Würth Elektronik eiSos Group, Germany

12:10 pm – 12:30 pm
ENHANCED RELIABILITY FOR POWER MODULES VIA A NEW AG/SI SINTER JOINING STRATEGY
Y. Liu[1], C. Chen[1], Koji S. Nakayama[1], Minoru Ueshima[2], Takeshi Sakamoto[2], Takuya Naoe[3], Hiroshi Nishikawa[3], Katsuaki Suganuma1
[1]Flexible 3D System Integration Laboratory, Osaka University, Japan; [2]Daicel Corporation, Japan; [3]Joining and Welding Research Institute, Osaka University, Japan

12:30 pm – 1:00 pm
Closing session - Awards

1:00 pm – 2:00 pm
Light Lunch & Exhibition

NETWORKING EVENTS

WELCOME RECEPTION

Monday 11 September 20233 at Homerton College, Cambridge
// 6:00 pm – 7:30 pm

We will be kicking off this year's conference with a welcome drinks and canapes reception at Homerton College. Don't miss the chance to get the lay of the land and meet the other conference delegates before heading into the hustle and bustle of the conference program. Afterwards you are free to choose from a selection of local restaurants within walking distance.

Sponsored by ASE

EXHIBITION, POSTER & PIZZA

Tuesday 12 September 2023 at the Genome Center
// 5:10 pm – 7:00 pm

Your chance to take a stroll around the exhibition booths and check out the posters as well. The presenters will be there to explain their research in detail and the exhibitors will be happy to answer your questions about their product and service portfolio. Oh, and there will be pizza and refreshments.

CONFERENCE DINNER

Wednesday 13 September 2023 at Homerton College, Cambridge
// 6:00pm- 10:00pm

A Conference Dinner has been organised at Homerton College Cambridge on Wednesday 13 September 2023, in the spacious, modern Dining Hall (picture of Exterior), where Conference Delegates will have the opportunity to network with fellow attendees and enjoy a three course meal and refreshments as part of the Conference ticket.

Sponsored by ASE

THANK YOU
TO ALL OUR SPONSORS AND EXHIBITORS

Besi

Accelonix keeping you ahead

PacTech member of nagase group

inseto ADVANCED TECHNOLOGY FOR RESEARCH & INDUSTRY

ASE · ALLIED HIGH TECH PRODUCTS, INC · AMADYNE GMBH · CS connected · Cupio SERVICES

DYCOTEC MATERIALS · Fraunhofer IZM · HONEYSTONE · saes industrial · set

SMART HIGH TECH · TORAY Innovation by Chemistry · capLINQ · CATAPULT Compound Semiconductor Applications · DELO INDUSTRIAL ADHESIVES

DISCO · eurofins | MASER · KOH YOUNG TECHNOLOGY · Kulicke & Soffa · MCS

SERMA MICROELECTRONICS · Surfx · ZEISS · ALTER · GEN3 PRECISION AS STANDARD · Megatech

MatchID Metrology beyond colors · ROARTIS IQ-BOND · OPTIM WAFER SERVICES · UNITEMP · VIA ELECTRONIC

Co-Sponsored by: IEEE · IEEE ELECTRONICS PACKAGING SOCIETY · iMAPS EUROPE

BOOTH PLAN

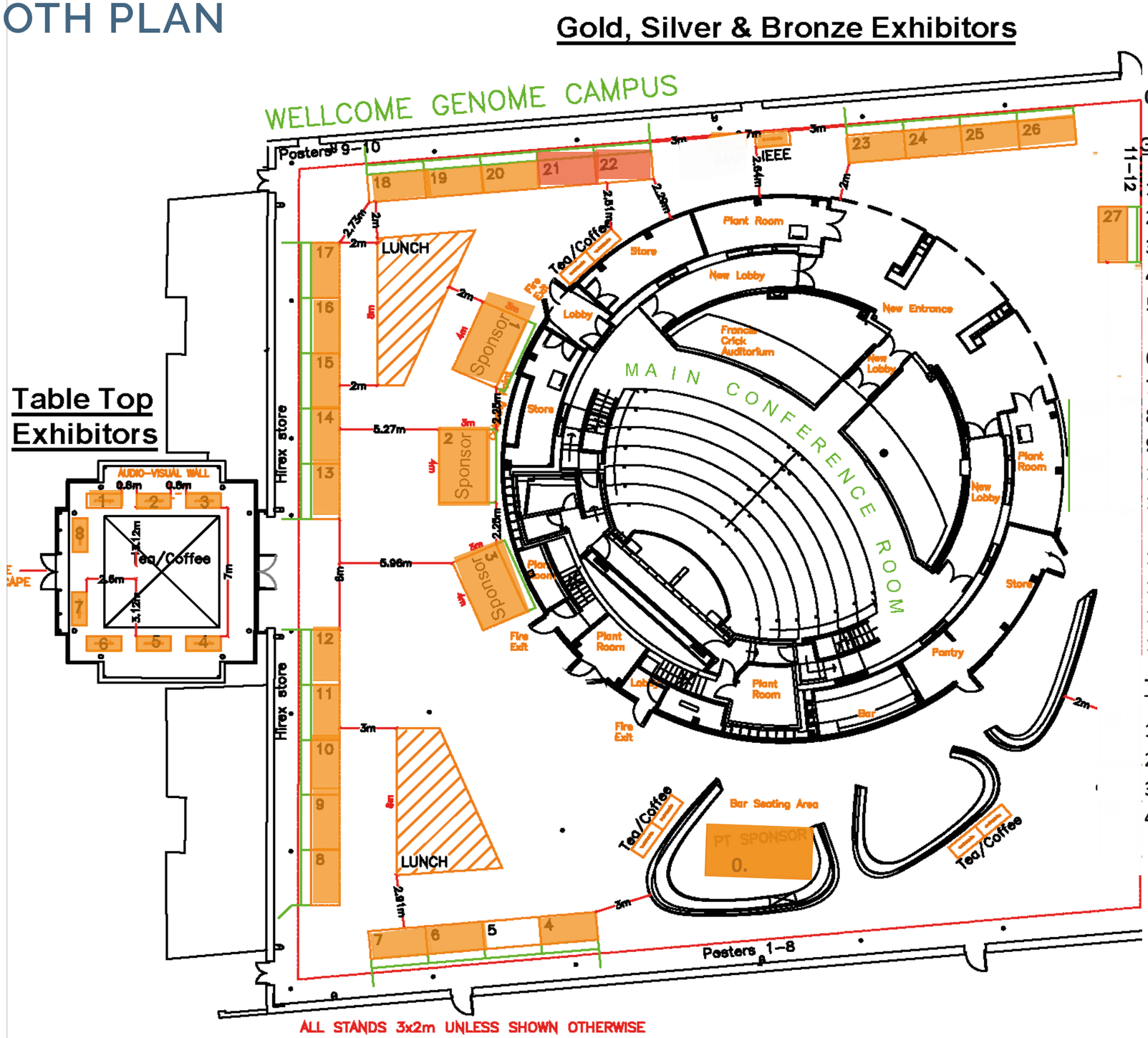


Table Top Exhibitors

Gold, Silver & Bronze Exhibitors

Platinum Sponsor

0. Besi

Gold, Silver & Bronze Exhibitors

1. inseto
2. PacTech
3. Accelonix
4. MCS
5. Allied High Tech Products
6. Dycotec
7. CSconnected
8. ASE
9. ZEISS
10. SAES
11. Eurofins MASER
12. DISCO
13. DELO
14. Cupio
15. Fraunhofer IZM
16. CSA Catapult
17. CAPLINQ
18. Kulicke & Soffa
19. Surfx Technologies
20. SERMA Microelectronics
21. Koh Young Technology
22. Amadyne
23. Honeystone
24. SET
25. Smart High Tech AB
26. IMAPS UK
27. Toray International

Table Top Exhibitors

1. Megatech
2. MatchID
3. Alter Technology
4. GEN3
5. UniTemp
6. Optim Wafer Services
7. Roartis
8. VIA electronic

PLATINUM, GOLD AND SILVER EXHIBITORS SHOWCASE

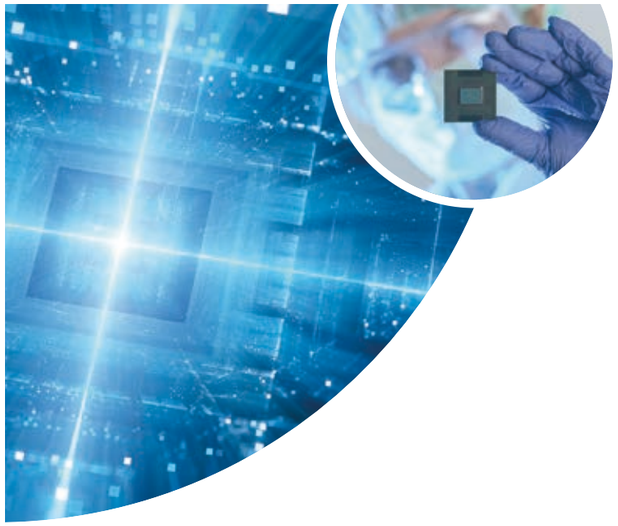
Besi

Besi is a leading supplier of semiconductor assembly equipment and develops cutting edge assembly processes and equipment for a variety of semiconductor applications.

Drivers of Innovation

Besi is proud to sponsor the EMPC 2023.

www.besi.com



inseto

ADVANCED TECHNOLOGY FOR RESEARCH & INDUSTRY

LEADING TECHNICAL DISTRIBUTOR
OF EQUIPMENT AND RELATED MATERIALS TO THE

MICROELECTRONIC AND **ADVANCED TECHNOLOGY** SECTORS

ADHESIVES

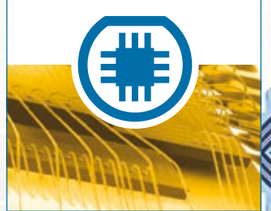
A comprehensive range of technical adhesives and sealants for the automotive, electronic and general manufacturing industries

EQUIPMENT

Providing fabrication, assembly and test equipment for research and production of semiconductor devices and related technologies

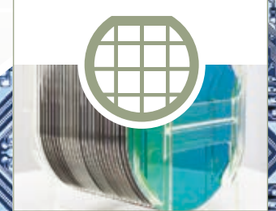
MATERIALS

For assembly materials and machine consumable products used in microelectronic, photonic and high-frequency devices



WAFERS

A wide range of wafers and substrates supplied worldwide, including silicon, compound semiconductor and glass materials



Call: +44 (0)1264 334505

enquiries@inseto.co.uk

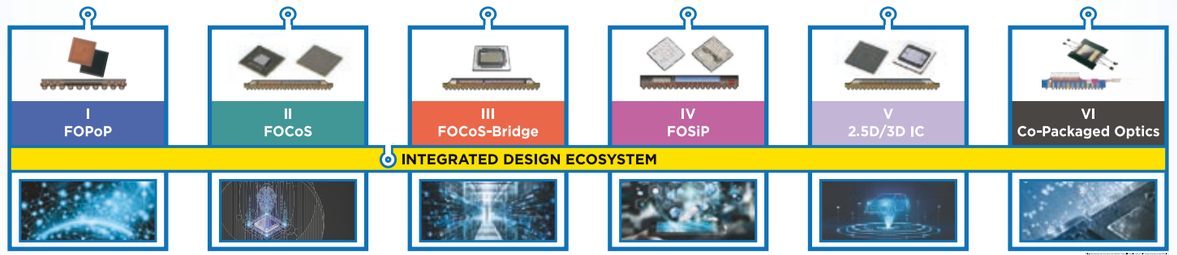
inseto.co.uk

ASE

The world's leading global provider of semiconductor manufacturing services in assembly and test introduces...

VIPack™

An advanced packaging platform designed to enable vertically integrated package solutions.



"Our expanding digitized world is driving unparalleled innovation across the semiconductor industry and VIPack™ represents a crucial leap forward in the transformational packaging technologies required to achieve the highly complex system integration our customers need to remain competitive," said Yin Chang, Senior Vice President of Sales and Marketing. "Through VIPack™, we're empowering our customers to discover new efficiencies in their semiconductor design and manufacturing process and to reimagine the integration technologies required to accomplish application excellence."

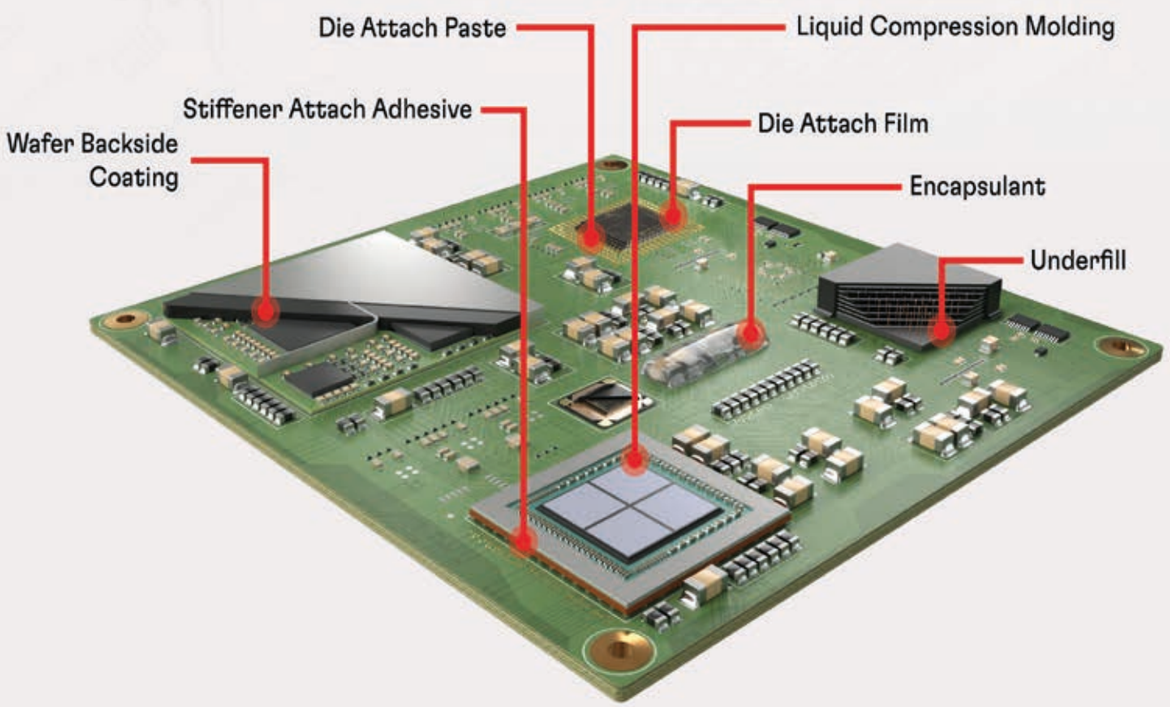
"ASE is delighted to bring its VIPack™ platform to market, opening up new opportunities for our customers to innovate from the design process all the way to production and to reap extensive benefits in relation to functionality, performance, and cost," said Dr. C.P. Hung, Vice President of R&D, ASE. "As the world's leading OSAT, ASE is strategically positioned to help customers improve efficiency, speed time-to-market, and sustain profitable growth. VIPack™ underscores our commitment to deliver our most innovative packaging technologies to date."

Available now, ASE's VIPack™ is a scalable platform that will expand in alignment with industry roadmaps

@aseglobal @aseglobal aseglobal.com

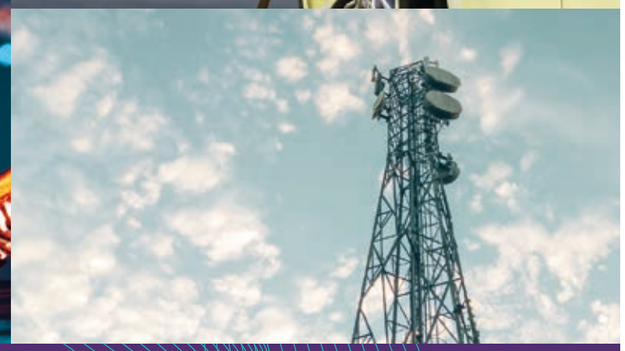
Henkel

capLINQ



ENABLING THE NEXT GENERATION OF SEMICONDUCTOR PACKAGING

Assembly Films | Conductive and Insulating Adhesives | Optically Clear Encapsulants | Polyimide Tapes | Bonding Wires | Solder Spheres | Thermal Interface Materials
Semiconductor Molding Compounds | Optoelectronic Molding Compounds | Surface Treatments | Leadframes | Semiconductor Mold Maintenance | Mold Release Sprays



Compound Semiconductor Applications (CSA) Catapult is the UK's authority on compound semiconductor applications and commercialisation.

CSA Catapult helps businesses solve the technical problems they face when taking their products and applications to market, using our expertise, know-how and state-of-the-art equipment.

Our diverse team of semiconductor and compound semiconductor packaging experts help businesses to develop next-generation technology across Power Electronics, RF & Microwave and Photonics through innovative package design, modelling, thermal management, assembly and testing.

CSA Catapult is home to the Driving the Electric Revolution Industrialisation Centre (DER-IC) for the South West and Wales. Our state-of-the-art 3D printing capability, unique to the UK, carries out multi-material, metal, and ceramic 3D packages, heat sinks, and embedded packaging.

Find out how we can help you:

csa.catapult.org.uk
collaboration@csa.catapult.org.uk

CSACatapult

Compound Semiconductor Applications (CSA) Catapult

CATAPULT
Compound Semiconductor Applications

UKRI Innovate UK

eurofins | MASER

FAILURE ANALYSIS & RELIABILITY TEST

FAILURE ANALYSIS

- Non-destructive Analysis
- Failure Localization
- Package Decapsulation
- FIB Circuit Edit
- DPA/Construction Analysis
- IPC-A-600/610 PCB Inspection
- Complete RMA flow

RELIABILITY TEST

- ESD & Latch Up Testing
- AEC-Q100 Qualification
- JEDEC Qualification
- System Level Testing
- Mechanical Testing
- Environmental Testing
- HALT Robustness Testing

Eurofins MASER B.V. | Auke Vleerstraat 26 | 7521PG Enschede | The Netherlands | www.maser.nl

Surfx Technologies

Atmospheric-Pressure Plasma Systems

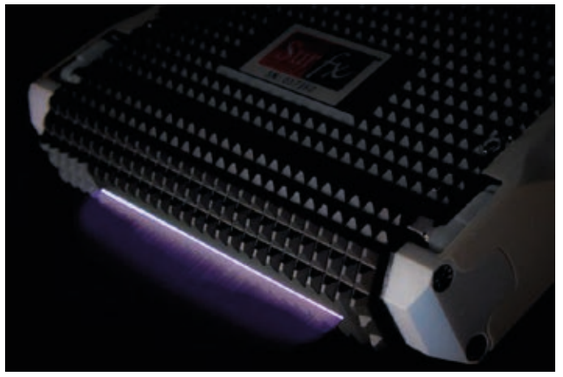
Surfx Technologies' atmospheric-pressure argon plasma systems are designed to clean and activate substrates for improved adhesion. They are ideal for semiconductor packaging and electronics manufacturing. Turnkey automated systems come standard with in-line conveyance for high-volume manufacturing. An optional drawer can be installed for high-mix, low-volume production. Integrator packages enable plasma cleaning inside bonders.

Surfx's Atomflo™ controller operates with low voltage, radio frequency (RF) power, and generates a uniform, particle free, and electrically neutral plasma that is safe on the most sensitive electronics.

Surfx plasma systems offer many options for in-line or batch manufacturing with full traceability:

- Oxygen plasma for organic clean
- Hydrogen plasma for metal oxide removal
- Cleanroom class 100 (10,000 is standard)
- Inert gas purge for reducing gas chemistry
- Substrate heating and cooling

For more information, contact Surfx at:
sales@surfxtechnologies.com or +1 310 558 0770.



Surfx®
The most trusted name in atmospheric plasma.™

STA-10iL Specifications

Work area (X * Y * Z)
550 x 760 x 60 mm

Footprint (W * D * H)
1,000 x 1,500 x 1,550 mm
39.4 x 59.1 x 61.0 inches

Software and OS
Cloudbreak™ for rapid program development.

Patented plasma technology
Atmospheric argon plasma
O_2, H_2, N_2 plasma chemistry
RF capacitive discharge

www.surfxtechnologies.com

North America
Surfx Technologies, LLC
Ph: +1 (310) 558-0770
sales@surfxtechnologies.com

Europe
Novel Technology Transfer GmbH
Ph: +49 8134 55700-12
Alex.Wanninger@novel-tec.de

CONTACT

EMPC 2023
Organised by:

IMAPS UK
125 High Street Chesterton
Cambridge CB4 1NL, UK
office@imaps.org.uk

Conference Chair:
Anne Vanhoestenberghe

Technical Chair:
Steve Riches

PCO
mcc Agentur für Kommunikation GmbH
Martina Creutzfeldt. Rahel Dietze & Ajda Omrani
Berlin, Germany
Phone: +49 30-61 28 86 11
office@empc2023.org
mcc-events.de

Co-sponsored by:

IEEE

IEEE ELECTRONICS PACKAGING SOCIETY

Organised by:

iMAPS UNITED KINGDOM